NON-VOLATILE MEMORY CELL SUITABLE FOR FLASH AND BYTE OPERATION APPLICATION

ABSTRACT OF THE INVENTION

The present invention provides a non-volatile memory cell structure suitable for the flash memory cell and EEPROM cell (electrically erasable programmable read only memory cell) to perform the byte programming and byte erase operations. In the programming operation, a higher negative voltage applied to the drain region, such that the hot hole is generated to induce the hot electron into the floating gate through the tunneling oxide layer in the lateral electrical field. In addition, the gate voltage is around the threshold voltage, which dependent on the integration circuit device design. Furthermore, the non-volatile memory cell utilized the channel Fowler-Nordheim tunneling for erasing operation. In order to perform the byte erasing operation, the drain junction used as an inhibition switch. Thus, the unselected cell in the same word line is inhibited by biasing the drain to ground. Therefore, the word lines of unselected cells are ground.